FAIRCHILD
SEMICONDUCTOR®

November 2009

FAN7083_GF085
High Side Gate Driver with Reset

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation up fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- dv/dt immune.
- Gate drive supply range from 10V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- High side output in phase with input
- $\overline{\text{RESET}}$ input is 3.3V and 5V logic compatible

Typical Applications

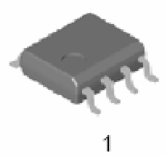
- Diesel and gasoline injectors/valves
- MOSFET-and IGBT high side driver applications

For Fairchild's definition of "green" Eco Status, please visit:
http://www.fairchildsemi.com/company/green/rohs_green.html

Description

The FAN7083_GF085 is a high-side gate drive IC with reset input. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to VS=-5V (typical) at VBS=15V. Logic input is compatible with standard CMOS outputs. The UVLO circuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 200mA and 400mA respectively, which is suitable for magnetic-and piezo type injectors and general MOSFET/IGBT based high side driver applications.

SOIC-8

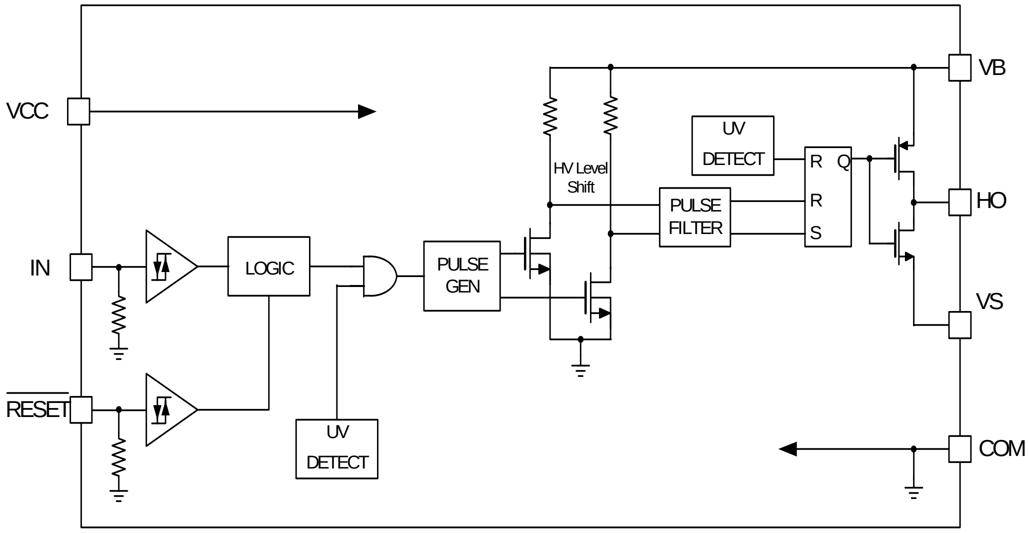


Ordering Information

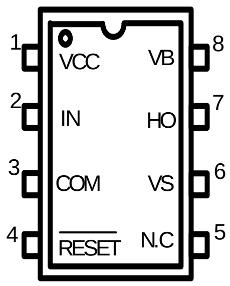
Device	Package	Operating Temp.
FAN7083M	SOIC-8	-40 °C ~ 125 °C
FAN7083MX	SOIC-8	-40 °C ~ 125 °C

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

Pine Number	Pin Name	I/O	Pin Function Description
1	VCC	P	Driver supply voltage
2	IN	I	Logic input for high side gate drive output, in phase with HO
3	COM	P	Ground
4	$\overline{\text{RESET}}$	I	Reset input
5	NC	-	NC
6	VS	P	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	VB	P	Driver output stage supply

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply offset voltage	V_S	V_B-25	V_B+0.3	V
High side floating supply voltage	V_B	-0.3	625	V
High side floating output voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Supply voltage	V_{CC}	-0.3	25	V
Input voltage for IN	VIN	-0.3	V_{CC}+0.3	V
Input voltage for $\overline{RESET}$	V_{RESET}	-0.3	V_{CC}+0.3	V
Power Dissipation [1)]	Pd		0.625	W
Thermal resistance, junction to ambient [1)]	Rthja		200	°C/W
Electrostatic discharge voltage (Human Body Model)	V_{ESD}	1K		V
Charge device model	V_{CDM}	500		V
Junction Temperature	Tj		150	°C
Storage Temperature	T_S	-55	150	°C

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;
JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural convection(StillAir)
JESD51-3 : Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.-40°C <= Ta <= 125°C

Parameter	Symbol	Min.	Max.	Unit
High side floating supply voltage -10V Transient 0.2us	V_B	V_S + 10	V_S + 20	V
High side floating supply offset voltage(DC)	V_S	-4 (@VBS >= 10V) -5 (@VBS >= 11.5V)	600	V
High side floating supply offset voltage(Transient)	V_S	-25 (~200ns) -20(200ns~240ns) -7(240ns~400ns)	600	V
High side floating output voltage	V_{HO}	V_S	V_B	V
Allowable offset voltage Slew Rate [1)]	dv/dt	-	50	V/ns
Supply voltage	V_{CC}	10	20	V
Input voltage for IN	V_{IN}	0	Vcc	V
Input voltage for $\overline{RESET}$	V_{RESET}	0	Vcc	V
Switching Frequency [2)]	Fs		200	KHz
Ambient Temperature	Ta	-40	125	°C

Note : 1) Guaranteed by design.
2) Duty = 0.5

Statics Electrical Characteristics

Unless otherwise specified, -40°C <= Ta <= 125°C, V_{CC} = 15V, V_{BS} = 15V, V_{RESET} = 5V, V_S = 0V, R_L = 50Ω, C_L = 2.5nF.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vcc and VBS supply Characteristics						
V_{CC} and V_{BS} supply under voltage positive going threshold	V_{CCUV+} V_{BSUV+}	-	-	9.0	9.8	V
V_{CC} and V_{BS} supply under voltage negative going threshold	V_{CCUV-} V_{BSUV-}	-	7.4	8.4	-	V
V_{CC} and V_{BS} supply under voltage hysteresis	V_{CCUVH} V_{BSUVH}	-	0.2	0.6	-	V
Under voltage lockout response time	tduvcc tduvbs	VCC: 10V-->7.3V or 7.3V-->10V VBS: 10V-->7.3V or 7.3V-->10V	0.5 0.5		20 20	us us
Offset supply leakage current	I_{LK}	V_B=V_S=600V	-	-	50	uA
Quiescent V_{BS} supply current	I_{QBS}	V_{IN}=0, V_{RESET}=5V	-	50	100	uA
Quiescent Vcc supply current	I_{QCC1}	V_{IN}=V_{RESET}=0	-	65	140	uA
Quiescent Vcc supply current	I_{QCC2}	V_{IN}=15V, V_{RESET}=0	-	75	160	uA
Input Characteristics						
High logic level input voltage for IN	V_{IH}	-	0.63Vcc		-	V
Low logic level input voltage for IN	V_{IL}	-	-	-	0.4Vcc	V
High logic level input current for IN	I_{IN+}	V_{IN}=15V	-	15	50	uA
Low logic level input bias current for IN	I_{IN-}	V_{IN}=0	-	0	1	uA
High logic level input voltage for $\overline{RESET}$	V_{RIH}	-	3.0	-	-	V
Low logic level input voltage for $\overline{RESET}$	V_{RIL}	-	-	-	1.4	V
High logic level input current for $\overline{RESET}$	I_{RIN+}	V_{RESET}=5V	-	5	30	uA
Low logic level input bias current for $\overline{RESET}$	I_{RIN-}	V_{RESET}=0	-	0	1	uA
Output characteristics						
High level output voltage, V_{BIAS}- VO	V_{OH}	I_O=0	-	-	0.1	V
Low level output voltage, VO	V_{OL}	I_O=0	-	-	0.1	V
Peak output source current	I_{O1+}	-	200	-	-	mA
Peak output sink current	I_{O1-}	-	400	-	-	mA
Equivalent output resistance	R_{OP}			54	75	Ω
	R_{ON}			24	38	Ω

Note: The input parameter are referenced to COM. The VO and IO parameters are referenced to COM.

Dynamic Electrical Characteristics

Unless otherwise specified, -40°C <= Ta <= 125°C, V_{CC} = 15V, V_{BS} = 15V, V_{RESET} = 5V, V_S = 0V, R_L = 50Ω, C_L = 2.5nF.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
IN-to-output turn-on propagation delay	t_{plh}	50% input level to 10% output level, V_S = 0V	-	115	250	ns
IN-to-output turn-off propagation delay	t_{phl}	50% input level to 90% output level V_S = 0V	-	90	200	ns
RESET-to-output turn-off propagation delay	t_{phl_res}	50% input level to 90% output level	-	90	200	ns
RESET-to-output turn-on propagation delay	t_{plh_res}	50% input level to 10% output level	-	115	250	ns
Output rising time	tr1	Tj=25°C,V_{BS}=15V	-	200	400	ns
	tr2		-	-	500	ns
Output falling time	tf1	Tj=25°C,V_{BS}=15V	-	25	200	ns
	tf2		-	-	400	ns

Application Information

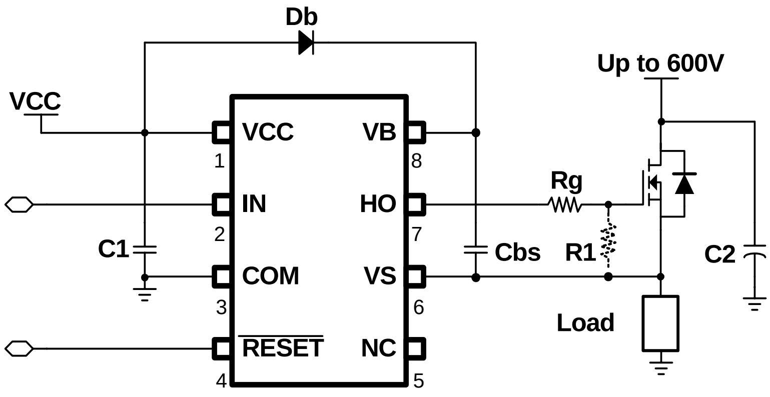
1. Relationship in input/output and supplies

VCC	VBS	$\overline{RESET}$	IN	HO
< VCCUVLO-	X	X	X	OFF
X	< VBSUVLO-	X	X	OFF
X	X	LOW	X	OFF
X	X	X	LOW	OFF
> VCCUVLO+	> VBSUVLO+	HIGH	HIGH	ON

Notes:

X menans independent from signal

Typical Application Circuit



Typical Waveforms

1. Input/Output Timing

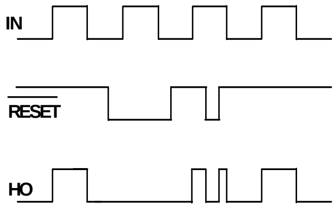


Figure 1a. Input/output Timing Diagram

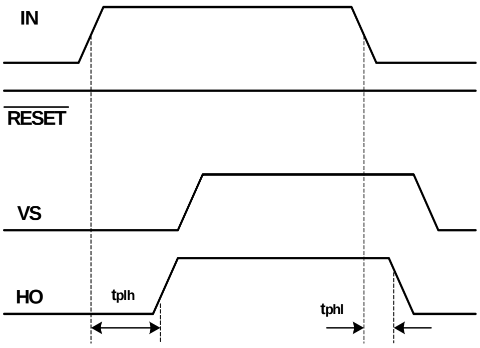


Figure 1b. Input(IN)/output Timing Diagram

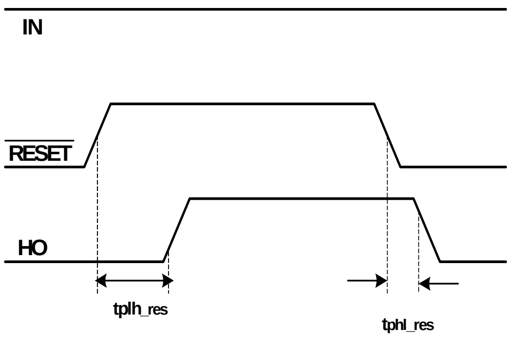


Figure 1C. Input($\overline{\text{RESET}}$)/output Timing Diagram

2. Ouput(HO) Switching Timing

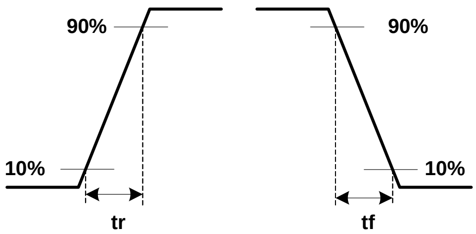


Figure 2. Switching Time Waveform Definitions

3.VB Drop Voltage Diagram

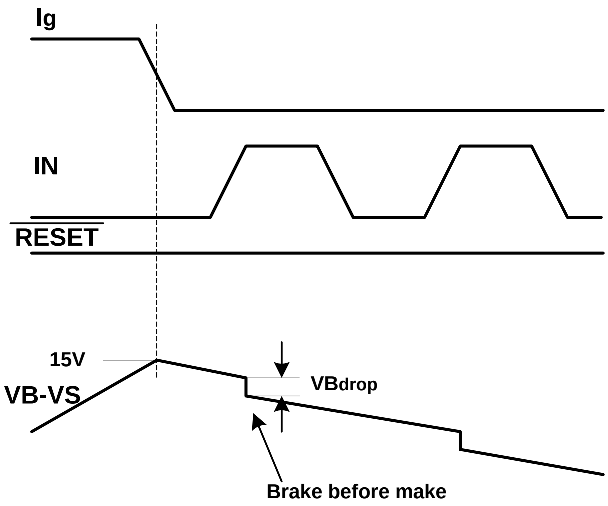


Figure 3a. VB Drop Voltage Diagram

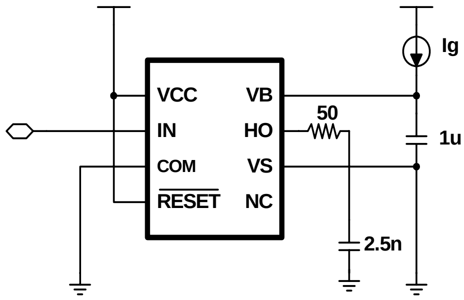


Figure3b. VB Drop Voltage Test Circuit

Performance Graphs

This performance graphs based on ambient temperature -40°C ~125°C

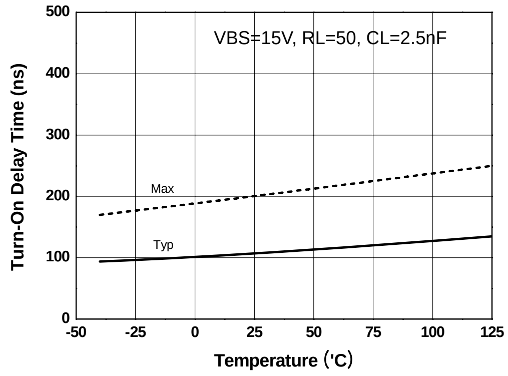


Figure 4a. Turn-On Delay Time vs Temperature

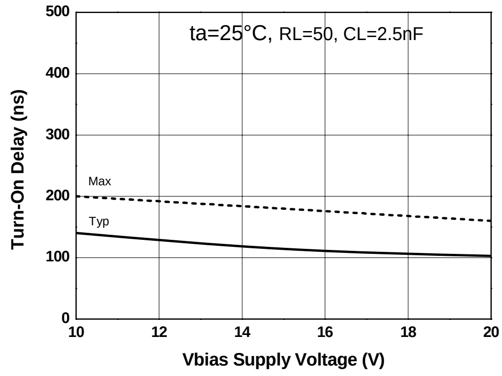


Figure 4b. Turn-On Delay Time vs VBS Supply Voltage

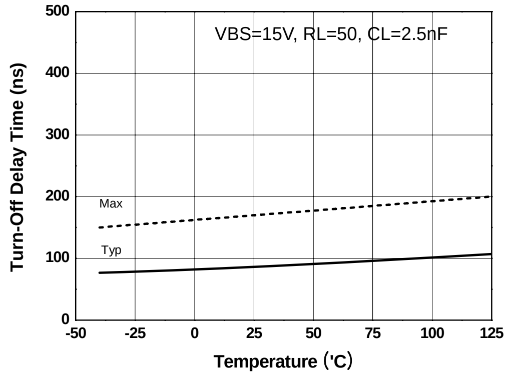


Figure 5a. Turn-Off DelayTime vs Temperature

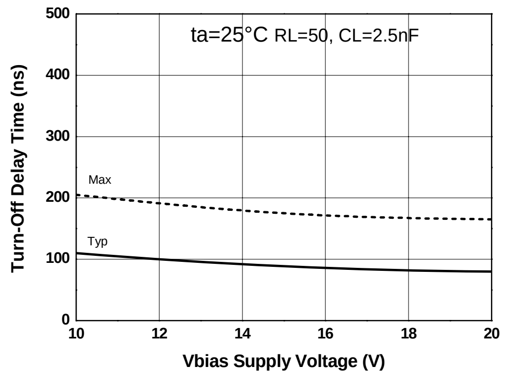


Figure5b. Turn-Off Delay Time vs VBS Supply Voltage

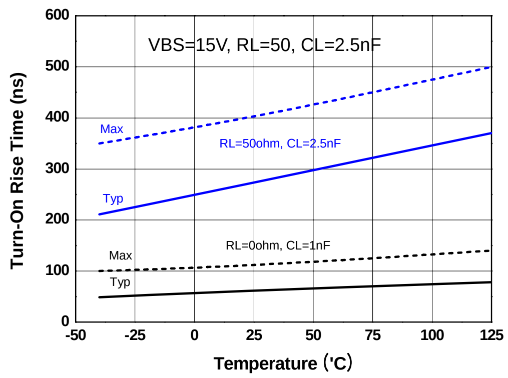


Figure 6a. Turn-On Rise Time vs Temperature

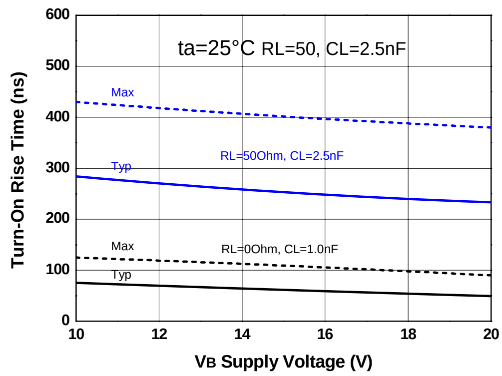


Figure 6b. Turn-On Rise Time vs VBS Supply Voltage

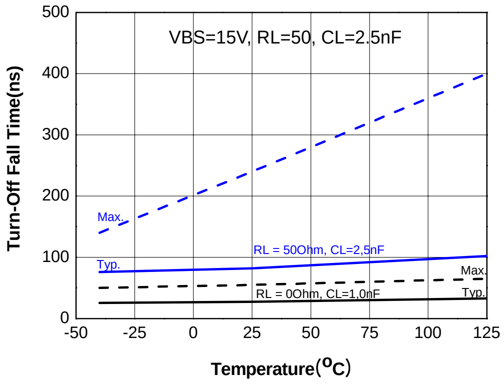


Figure 7a. Turn-Off Falling Time vs Temperature

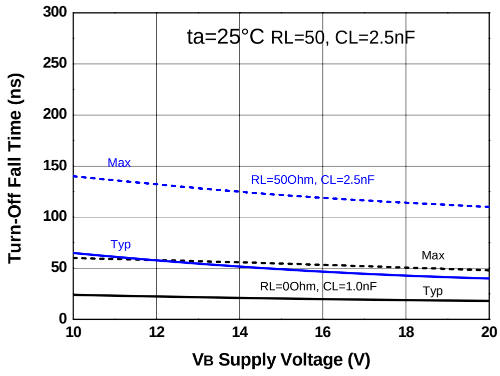


Figure 7b. Turn-Off Falling Time vs VBS Supply Voltage

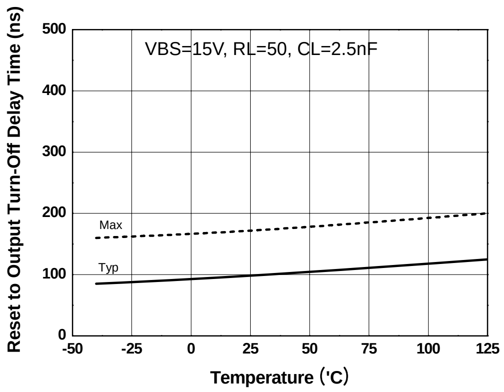


Figure 8a. RESET to output Turn-Off Delay Time vs Temperature

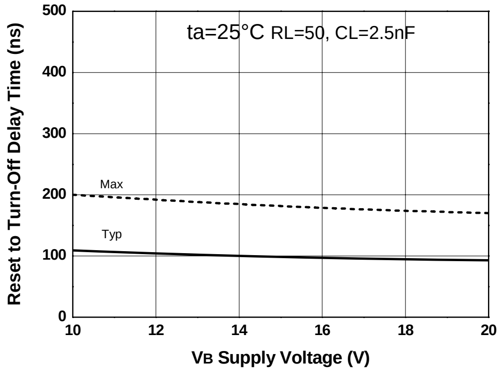


Figure 8b. RESET to output Turn-Off Delay Time vs VBS Supply

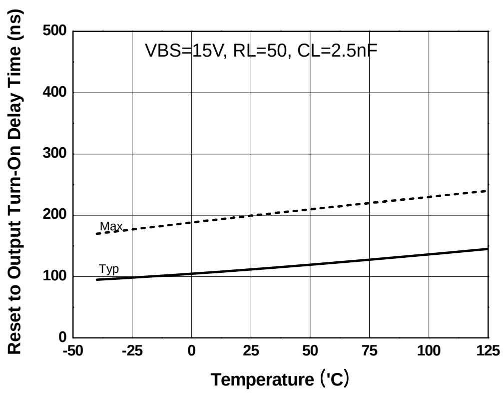


Figure 9a. RESET to output Turn-On Delay Time vs Temperature

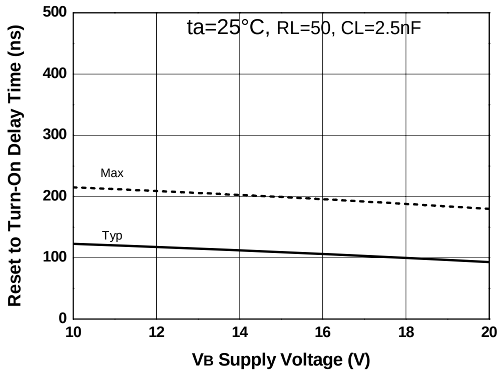


Figure 9b. RESET to output Turn-On Delay Time vs VBS Supply

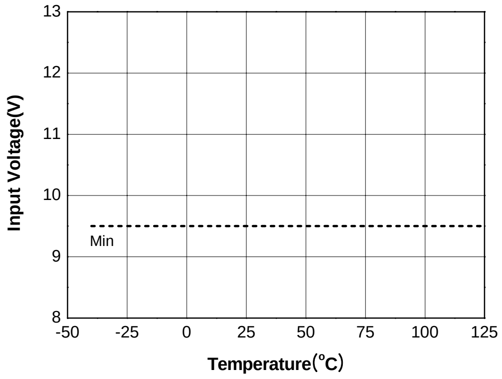


Figure 10a. Logic “1” IN Threshold vs Temperature

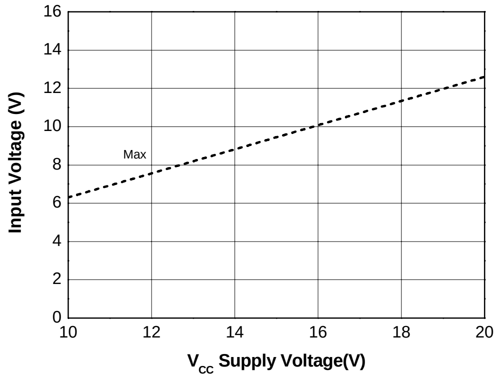


Figure 10b. Logic “1” IN Threshold vs VCC Supply Voltage

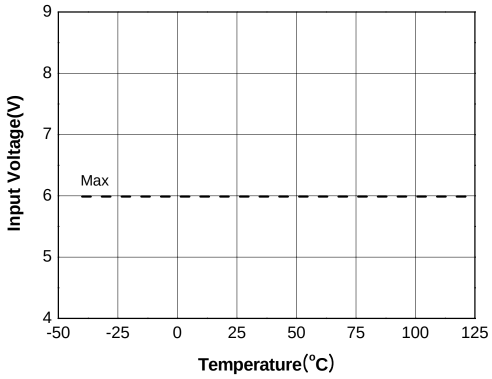


Figure 11a. Logic “0” IN Threshold vs Temperature

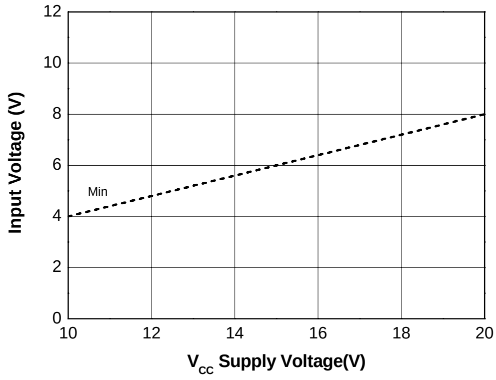


Figure 11b. Logic “0” IN Threshold vs VCC Supply Voltage

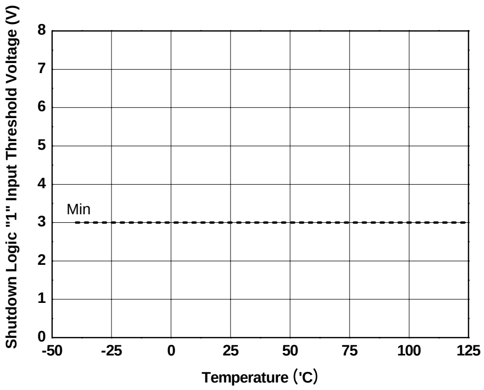


Figure 12a. Logic “1” Reset Threshold vs Temperature

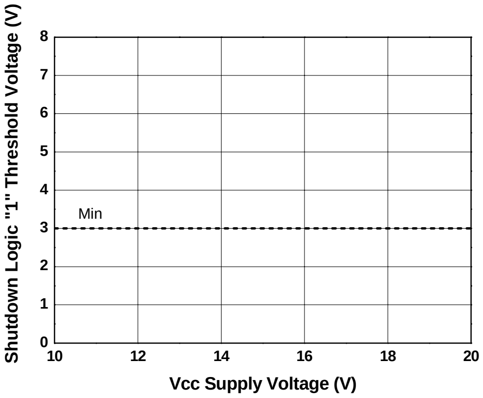


Figure 12b. Logic “1” Reset Threshold vs VCC Supply Voltage

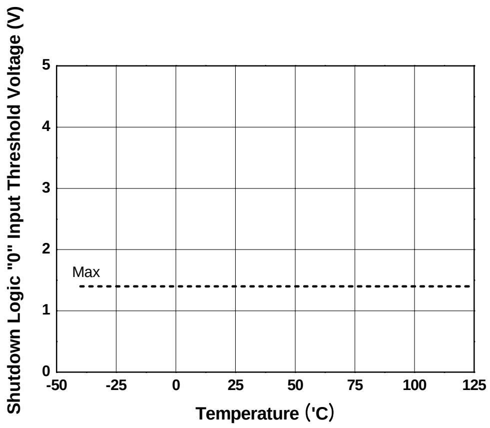


Figure 13a. Logic “0” Reset Threshold vs Temperature

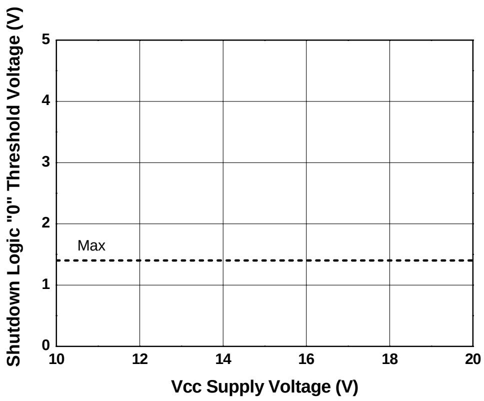


Figure 13b. Logic “0” Reset Threshold vs VCC Supply Voltage

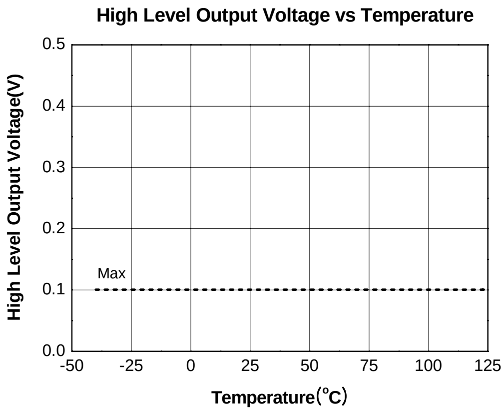


Figure 14a. High Level Output vs Temperature

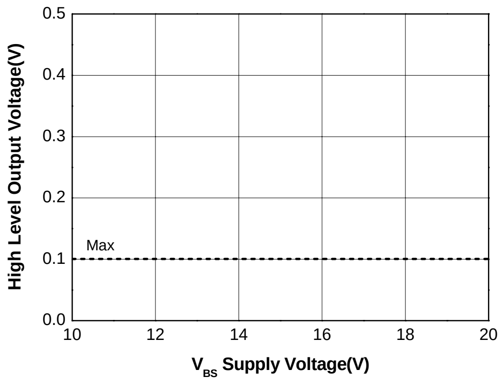


Figure 14b. High Level Output vs VBS Supply Voltage

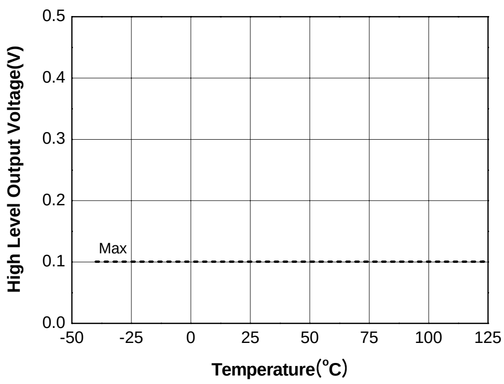


Figure 15a. Low Level Output vs Temperature

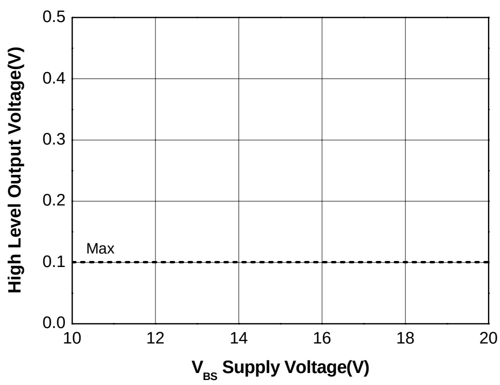


Figure 15b. Low Level Output vs VBS Supply Voltage

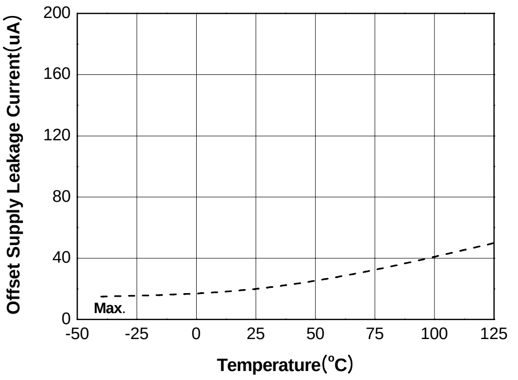


Figure 16a. Offset Supply Leakage vs Temperature

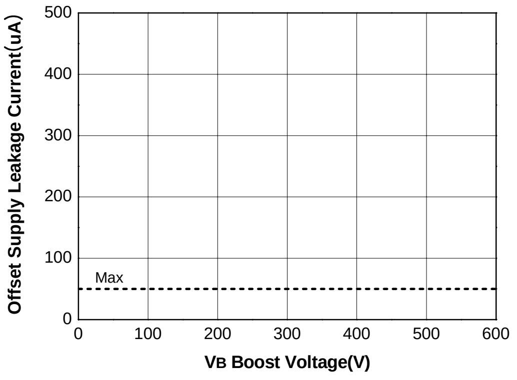


Figure 16b. Offset Supply Leakage vs Voltage

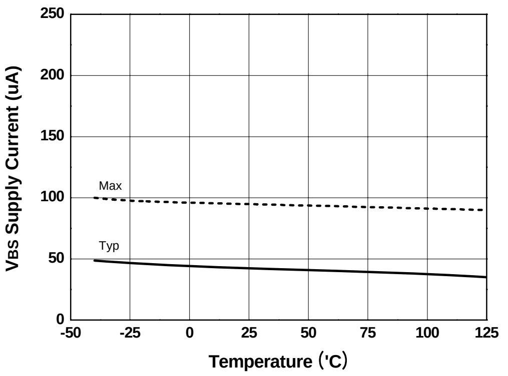


Figure 17a. VBS Supply Current vs Temperature

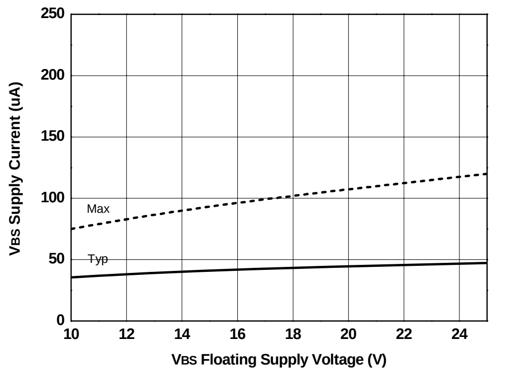


Figure 17b. VBS Supply Current vs VBS Supply Voltage

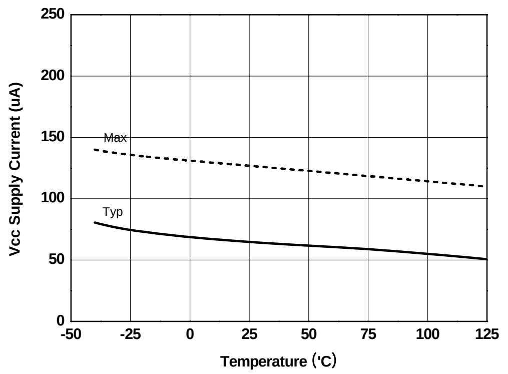


Figure 18a. VCC supply Current vs Temperature

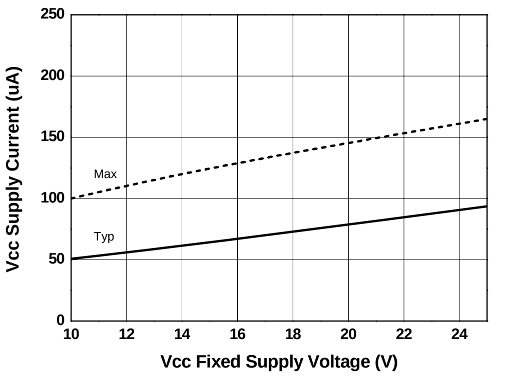


Figure 18b. VCC supply Current vs VCC Supply Voltage

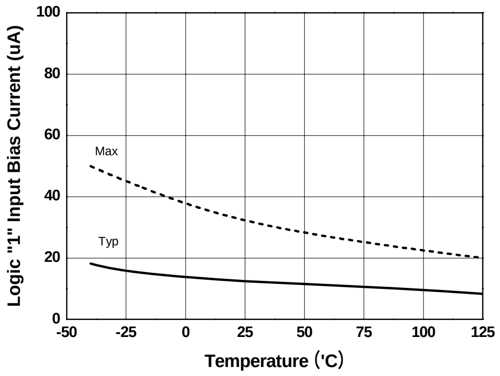


Figure 19a. Logic “1” IN Current vs Temperature

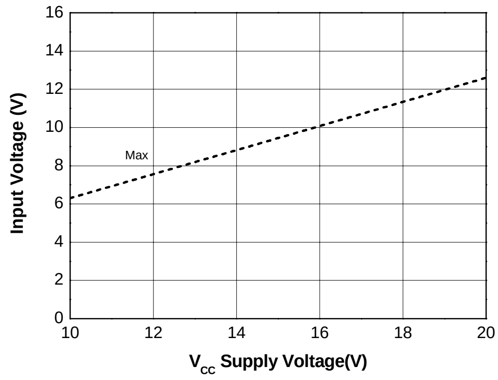


Figure 19b. Logic “1” IN Current vs Voltage

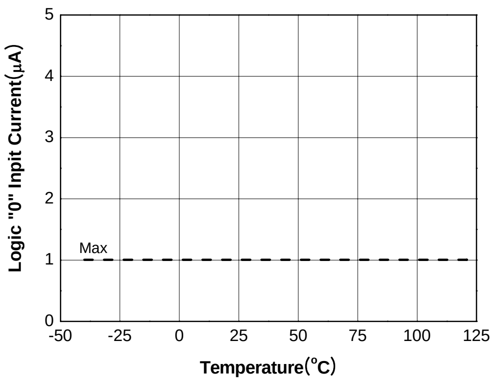


Figure20a. Logic “0” IN Current vs Temperature

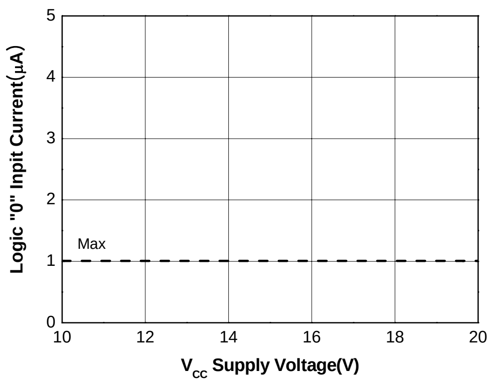


Figure 20b. Logic “0” IN Current vs Voltage

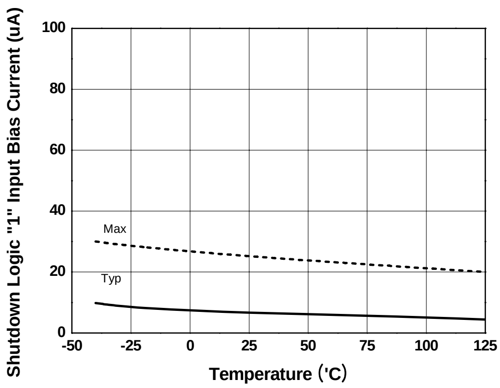


Figure 21. Logic “1” Reset Current vs Temperature

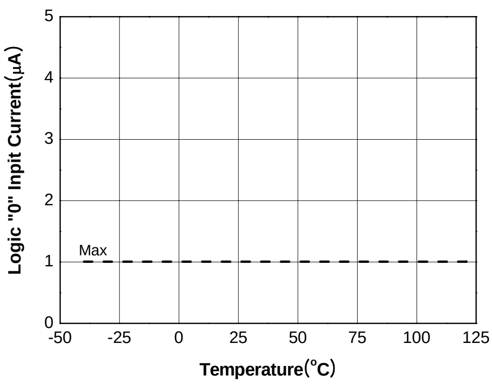


Figure 22. Logic “1” Reset Current vs Temperature

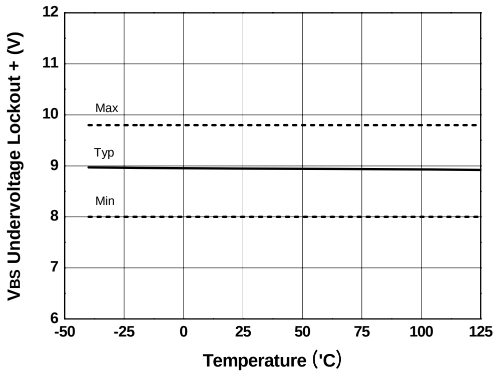


Figure 23a. VBS Undervoltage(+) vs Temperature

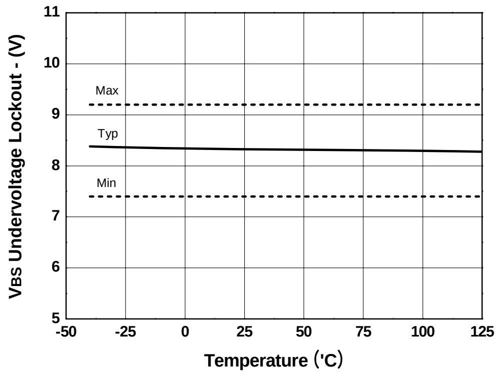


Figure 23b. VBS Undervoltage(-) vs Temperature

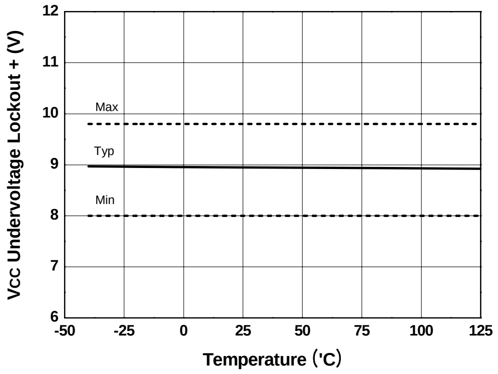


Figure 24a. VCC Undervoltage(+) vs Temperature

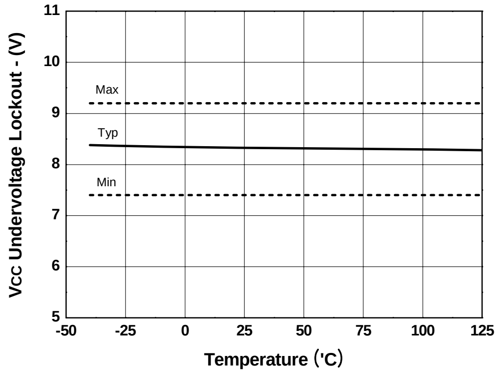


Figure 24b. VCC Undervoltage(-) vs Temperature

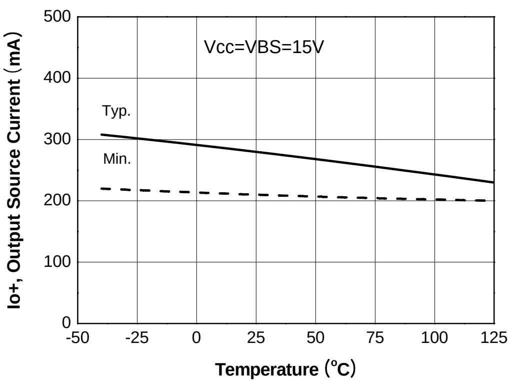


Figure 25a. Output Source Current vs Temperature

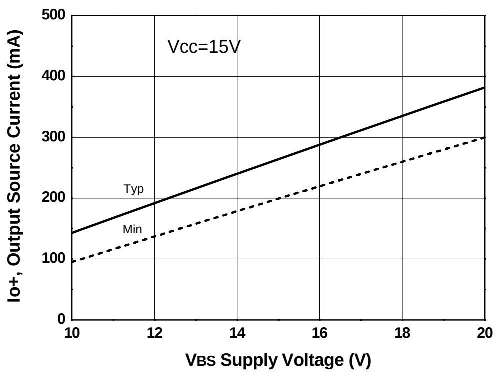


Figure 25b. Output Source Current vs Voltage

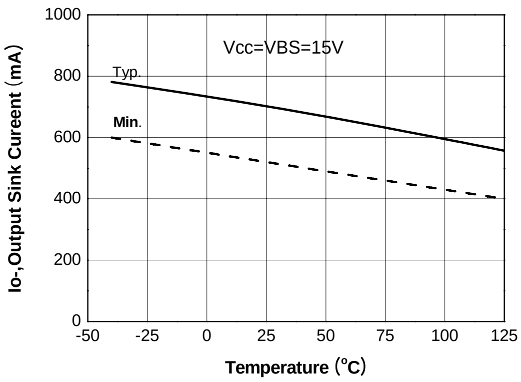


Figure 26a. Output Sink Current vs Temperature

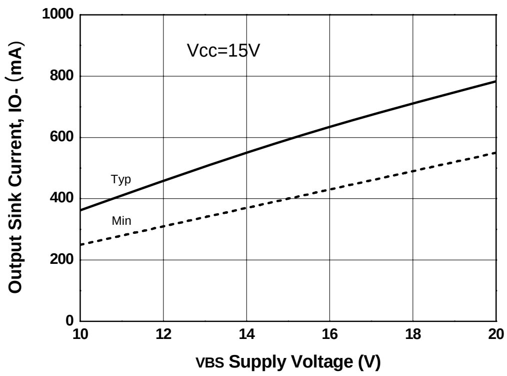


Figure 26b. Output Sink Current vs Voltage

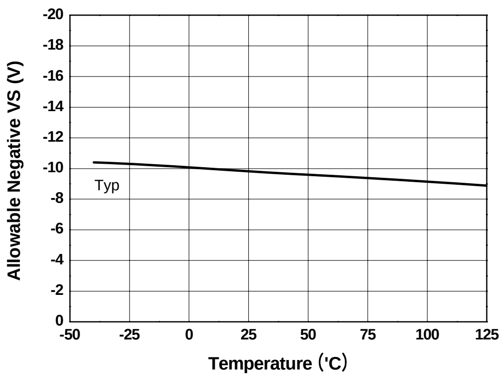


Figure 27a. Negative Allowable Offset vs Temperature

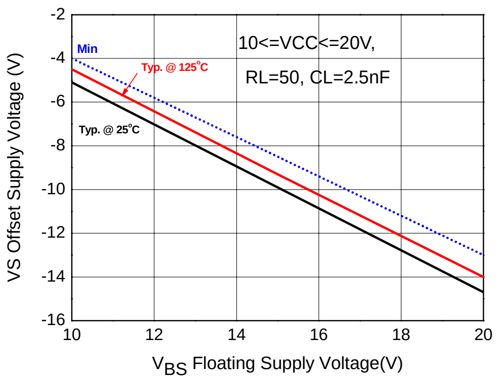


Figure 27b. Negative Allowable Offset vs Voltage

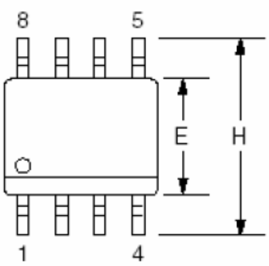
Package Dimensions

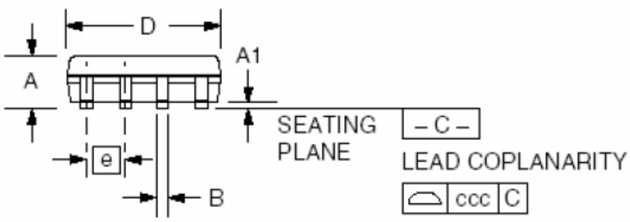
8-SOP

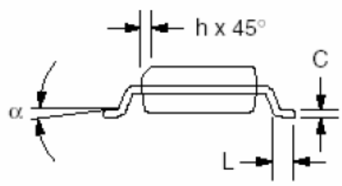
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







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Rev. I43